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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,227	09/16/2003	Kangguo Cheng	FIS920030221US1	2226

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INTERNATIONAL BUSINESS MACHINES CORPORATION
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EXAMINER	
ROSE, KIESHA L	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 03/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,227	CHENG ET AL.	
	Examiner	Art Unit	
	Kiesha L. Rose	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the amendment filed 29 November 2004.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 13,15-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Agahi et al. (U.S. Patent 6,335,239) in view of Hummler et al. (U.S. Patent 6,586,300).

Agahi discloses a DRAM (Fig. 2b) that contains a semiconductor wafer (203), a wafer having a trench etched through, an isolating collar (210) formed within the trench, a lower contact (218) for the vertical transistor formed above the collar, a vertical body layer of silicon (P-epi) formed on an exposed vertical surface within the trench where the exposed vertical surface being recessed transversely from an original trench width and extending upward substantially at original trench width and under a overhang of a pad dielectric (242), a gate dielectric (gate ox), formed on an exposed vertical surface of the silicon body layer within the trench, thereby isolating the body layer from the trench interior, a gate electrode (N+ Poly) formed within the trench an separated from the body layer of silicon by the gate dielectric layer, an upper electrode (220) formed in contact with the body layer of silicon thereby establishing a path for conducting carriers from the

lower contact to the upper contact through the vertical body layer, the gate electrode extending up to a wafer surface thereby leaving a central gate electrode ((N+ Poly (under WL conductor)) of width less than original trench width and having at least one aperture adjacent thereto that extends outward to the original trench width and down to make contact with the upper electrode and dielectric (OX) filling aperture adjacent to the central gate electrode to isolate central gate electrode, the central gate electrode capped by a gate contact cap (WL Conductor) and bracketed by gate contact sidewalls (Oxide) and an aperture (282) for a drain contact (232) formed adjacent to one of the gate contact sidewalls and being located transversely with respect to central gate electrode to make contact with said vertical body layer and with said drain, a capacitor (204/206) formed within a lower portion of the trench. Agahi discloses all the limitations except for a SiGe alloy on substrate. Whereas Hummler discloses a DRAM (Fig. 10) that contains a SiGe wafer above a bulk substrate, a trench etched through the SiGe layer into substrate, an isolating collar (120) formed within the trench, a lower contact (122) for the vertical transistor formed above the isolating collar and being in contact with a portion of the SiGe layer, a gate dielectric layer (154) formed on the exposed vertical surface of the trench, a gate electrode (156), a capacitor (124) formed within the lower portion of the trench, an isolating layer (131) formed within the trench overlapping vertically the lower contact thereby separating capacitor from the upper portion of the trench. The wafer was a SiGe layer to act as a workplace for a DRAM device to be formed. (Column 4, lines 24-35) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Agahi

by incorporating a SiGe wafer layer to act as a workplace for a DRAM device as taught by Hummler.

Claims 14 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Agahi and Hummler as applied to claims 13 and 19 above, and further in view of Imai et al. (U.S. Patent 5,847,419).

Agahi and Hummler disclose all the limitations except for a SiGe buffer layer formed between the substrate and a fully relaxed SiGe layer. Whereas Imai discloses a semiconductor device (Fig. 3d) that contains a substrate (11), a SiGe buffer layer (12) and a SiGe layer (15) formed thereon. The buffer layer is SiGe between the substrate and other SiGe layer to form tensile strain and improve higher speed. (Column 4, lines 48-65) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the devices of Agahi and Hummler by incorporating the SiGe buffer layer between the substrate and other SiGe layer to form tensile strain and improve higher speed as taught by Imai.

Response to Arguments

Applicant's arguments filed 29 November 2004 have been fully considered but they are not persuasive. Applicant's argued that the Agahi and Hummler reference do not disclose a strained silicon layer, whereas with the combination of the references a strained silicon layer is formed. The Agahi reference has a silicon vertical body layer and with the combination of the SiGe layer of Hummler with the two of them together it produces a strained silicon layer. In regards to the argument about the silicon layer not

recessed from the original trench width, the silicon layer is under the trench width and is not aligned with the pad nitride (242) and the layer (203) so the layer is recessed in the trench. Referring to the argument about the SiGe layer of Imai not being relaxed it is disclosed in the reference that the SiGe layer is in a relaxation condition and what is not relaxed is the substrate. (Column 4, lines 55-57) Therefore the rejections stand.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kiesha L. Rose whose telephone number is 571-272-1844. The examiner can normally be reached on M-F 8:30-6:00 off 2nd Mondays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KLR

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER